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10/644,215	08/20/2003	Darel N. Emmot	10001763-1	5465

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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,215	EMMOT ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The response filed 11/16/05 has been considered in preparing this office action.

Regarding claim 11, "**at the** at the" is repeated and should be –at the--.

Regarding claim 12, the claim depends from "claim 15" should be "claim 7".

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "partitioning logic" (claims 7 and 10-11) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed "the partitioning logic is located in at the subsystem" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed. The specification merely teaches "the chip set 218 in the Fig. 3 may be configured to partition the ..."(par 029) where the chip set 218 is not located in at the subsystem.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al (6,801,202 hereinafter "Nelson") in view of Spencer (6,311,247).

Nelson teaches a computer system (Figs. 2 and 3) comprising a host processor (102) configured to execute a single-threaded application; partitioning logic (such as, control unit 140 for dividing the stream of data received from computer system 80 into a corresponding number of parallel stream, col. 9, lines 20-24; and Fig. 22) for partitioning the state-sequenced information, communication logic (not shown, but can be any bus connectivity logic, such as, crossbar, chipset or bridge, see col. 8, lines 13-20, such as, arbiter in control unit of Fig. 22) configured to communicate partitioned state-sequenced information across a plurality of I/O busses (shows one bus, but could be multiple separate busses since Nelson suggests one or more graphics processor 90, see col. 9, line 1, further see Spencer for the teachings of multiple busses); a plurality of interfaces (bus arbiter) located at a subsystem (112) for receiving the information communicated across the plurality of I/O busses; processing logic (graphics processor 90 in Fig. 3) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed. However, Nelson fails to explicitly teach a plurality of I/O busses. This is what Spencer teaches. Spencer teaches a computer system (Fig. 2) comprising a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information, communication logic (chipset 120) configured to communicate partitioned state-sequenced information across a plurality of I/O busses (PCI buses 116-118); a plurality of interfaces (124-128)

located at a subsystem for receiving the information communicated across the plurality of I/O busses; processing logic (not shown, but would have been obvious to connect any peripheral (I/O) devices into the PCI busses 116-118, for example, graphics processor is considered one of the peripheral device) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of separate multiple I/O or PCI busses into the system of Nelson in order to replace the single bus system of Nelson by the multiple busses of Spencer because multiple separate busses allows exclusive communication by providing a direct pipe therebetween and thus provides significant performance enhancements over prior art systems that have shared PCI busses as taught by Spencer (abstract). Therefore, at least claims 7, 9, 10, 12 and 14 would have been obvious.

As per claim 8, Spencer teaches a buffer memory (Fig. 4, cache 150) in communication with the host processor for storing state-sequenced information for communication to a subsystem.

As per claim 11, Spencer teaches the partitioning logic is located in at the host processor (Fig. 2, chipset 120).

As per claim 13, Nelson teaches the processing logic comprises at least one geometry accelerator (112).

As per claim 15, the combined system teaches the system comprises a plurality of processing nodes that are coupled through a communication network (Nelson, one or more graphics processor, col. 9, line 1 and Spencer, PCI devices connect into the PCI busses 116-118).

Method claims 1, 2 and 4-6 are similar in scope to system claims 7-15 above, and thus are rejected under similar rationale.

As per claim 3, Nelson teaches the communicating partitioned state-sequenced information comprises performing at least one DMA across each of the plurality of I/O busses (col. 8, lines 26-31).

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al (6,801,202 hereinafter "Nelson") and Spencer (6,311,247) as applied to claims 7 and 15 above, and further in view of Ebihara et al (6,924,807 hereinafter "Ebihara").

The teachings of Nelson and Spencer are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach the processing logic comprises work queues maintained among the processing nodes. This is what Ebihara teaches. Ebihara teaches an image processing apparatus comprising a plurality of graphics processors (104), each being operable to render the image data (110) and at least one merge unit (106) operable to synchronously (108 or 118) receive the image data and synchronously (108 or 118) produce combined frame image data based thereon (abstract, Fig. 3). The Synchronous unit (108) performs similar functions as the work queue which provides synchronization among plurality of graphics processor. It would have been obvious to one of ordinary skill in the art at the time the

present invention was made to combine the synchron unit (108 or 118) into the combined system in order to provide synchronization among multiple graphics processors and thus to provide synchronized output signals. Therefore, at least claim 16 would have been obvious.

Response to Arguments

7. Applicant's arguments filed 11/16/05 have been fully considered but they are not persuasive.

Regarding objection to the drawings, since the claims particular require a "partitioning logic" which is a device within the chip set 218. Applicant better put this device into the chip set in order to fully compliance with the all the statutes and regulations.

Regarding 35 USC 103 rejections, applicant argues ""there is no teaching in Spencer of the host processor being "configured to execute a single-threaded application." It is noted that even though Spencer is silent on whether the application being executed on the host processor is a single-threaded or multi-threaded application, it would have been obvious to one of ordinary skill in the art to implement Spencer because both single-threaded or multi-threaded provides advantages and for example, multi-threaded improves responsiveness, fast application and prioritization compares to single-threaded and single-threaded is slower and results in system idle time and user frustration. Furthermore, Nelson also teaches single-threaded applications.

Applicant further argues that Spencer fails to teach the "partitioning logic". The examiner disagrees. Spencer clearly suggest that "I/O controller 123 generally operates

to **parse and reformat the signals carried on bus 125 into much smaller units** that may be communicated over a high-speed bus comprising much fewer conductors." (col. 5, lines 15-19). Furthermore, Nelson teaches the controller 140 may also divide the stream of data received from computer system 80 into a corresponding number of parallel streams that are routed to the individual rendering units 150A-D (col. 9, lines 20-24).

Applicant also argues that Spencer fails to teach the claimed "processing logic" and each of the PCI devices of Spencer performs its operations independently of the other PCI devices and therefore would have no reason or need to re-sequence any state-sequenced information because information sent to a disc driver controller (one of the PCI devices), would not be linked, in a state-sequenced fashion, with information sent to devices like video card**s**. The examiner agrees. However, the information sent to one of the video cards (one of the PCI devices), would be linked, in a state-sequenced fashion, with information sent to other video card**s**. It is noted that there are more than one video cards. Also, Nelson teaches processing logic (rendering units 150A-D and sample-to-pixel calculation unit 170A-D).

Then, applicant argues that claim 2 further requires "obtaining state information from the received information, and processing the information in a proper state context" which would have been obvious in view of the teachings of processing logic of Spencer and Nelson because both the processing logic receiving information from host computer and processing the data based on the information (data and command) received from the host computer.

Regarding prior art to Nelson, applicant argues that Nelson merely teaches a single high speed bus interface to the host computer, not multiple I/O busses. This may be correct. However, Nelson teaches multiple internal bus which communicates partitioned information from control unit 140 to the plurality of rendering units 150A-D where each bus communicates 1/nth of the total information (n is the number of rendering unit). Furthermore, Spencer teaches multiple I/O bus (such as, PCI busses).

It is noted that basically, applicant argues the non-obviousness by attacking references individually where, as here the rejections are based on combination of referencers. *In re Keller*, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the examiner clearly provided proper motivations to combine the multiple I/O busses of Spencer into the single I/O bus of Nelson as recited in the detail rejections above. Furthermore, Spencer clearly teaches the motivation to replace a shared single bus by multiple individual busses in order to provide significant performance enhancements over the prior art systems that have shared PCI buses - multiple PCI devices per PCI bus (see abstract).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671